0.18 µm Process Family:

XH018

0.18 Micron Modular Analog Mixed HV Technology

MIXED-SIGNAL FOUNDRY EXPERTS

DESCRIPTION

The XH018 series is X-FAB's 0.18 micron Modular Mixed Signal HV CMOS Technology. Based upon the industrial standard single poly with up to six metal layers 0.18 micron drawn gate length N-well process, integrated with high-voltage and Non-Volatile-Memory modules, the platform is ideal for SOC applications in the automotive market, as well as emdedded high-voltage applications in the communications, consumer and industrial market.

Comprehensive design rules, precise SPICE models, analog and digital libraries, IPs and development kits support the process for major EDA vendors.

KEY FEATURES OVERVIEW

- 0.18-micron single poly, up to six-metal N-well CMOS basic process
- Modular concept
- Up to 175°C operating temperature, extending beyond AEC Q100 requirement
- Low Power core module
- Thick metal layers optional module
- Integrated digital, analog, HV and NVM in a single process
- High-reliability NVM using SONOS technology
- Isolation well for all 1.8V, 3.3V and 40V MOS devices
- **NEW Primitive Devices:**
  - Low Vt Transistors
  - High capacitance single, double, triple MIM capacitors
  - Fringe capacitors
  - Photo diodes
- Integrated high-ohmic poly resistor in core module (zero mask penalty)
- 10-45V sym./asy. HVMOS transistors
- 35-45V DMOS transistors
- Vertical NPN BJT,
- ESD protected HV PNP for reverse polarity protection (e.g. for LIN pins)
- Single, double, triple MIM and Sandwich Capacitors
- Schottky & protection diodes
- Excellent Ron in HVMOS module with multiple resurf technology
- Very low mask count for an integrated analog process with HV and NVM
- Very low cost-per-function
- Various types of memory compiler (e.g. RAM, ROM, NVRAM, TrimOTP)
- High density up to 125000 gates per mm^2
- Typical and worst-case models (MOS, BJT, RES, CAP)
- MOS 1/f noise characterized & included in model
- Assura verification deck
- Common-Timing-Engine in Cadence P&R encounter platform
- Cadence & Mentor Graphic PDK

APPLICATIONS

- High temperature mixed-signal embedded systems/ system-on-chip (SOC)
- Automotive
- Analog frontends for sensors
- High precision mixed signal circuits
- Embedded high-voltage applications
- Power management IC
- Communications, Consumer and Industrial markets

QUALITY ASSURANCE

X-FAB spends a lot of effort to improve the product quality and reliability and to provide comprehensive support to the customers. This is maintained by the direct and flexible customer interface, the reliable manufacturing process and complex test and evaluation conceptions, all of them guided by strict quality improvement procedures developed by X-FAB. This comprehensive, proprietary quality improvement system has been certified to fulfill the requirements of the ISO 9001, QS 9000, VDA 6, ISO TS 16949 and other standards.

DELIVERABLES

- PCM tested wafers
- Optional engineering services: Multi Project Wafer (MPW) and Multi Layer Mask Service (MLM)
- Optional design services: feasibility studies, Place & Route, synthesis, custom block development

DIGITAL LIBRARIES

- Foundry-specific optimized libraries
- Low power, low leakage library for energy effecient and small size digital blocks
- Junction isolated library for low noise applications
- Multi-voltage library for multi-voltage and power cut-off applications
- Liberty™ synthesis models
- IEEE 1364 Verilog simulation models
- IEEE 1076.4 VHDL-VITAL simulation models

ANALOG LIBRARIES

- Operational Amplifiers
- Bias Cells
- Digital-to-Analog Converters
- Analog-to-Digital Converters
- RC Oscillators
- Power-On/Off-Reset
- Comperators
- Bandgaps
- Voltage Regulators
- Over-Temperature Detector

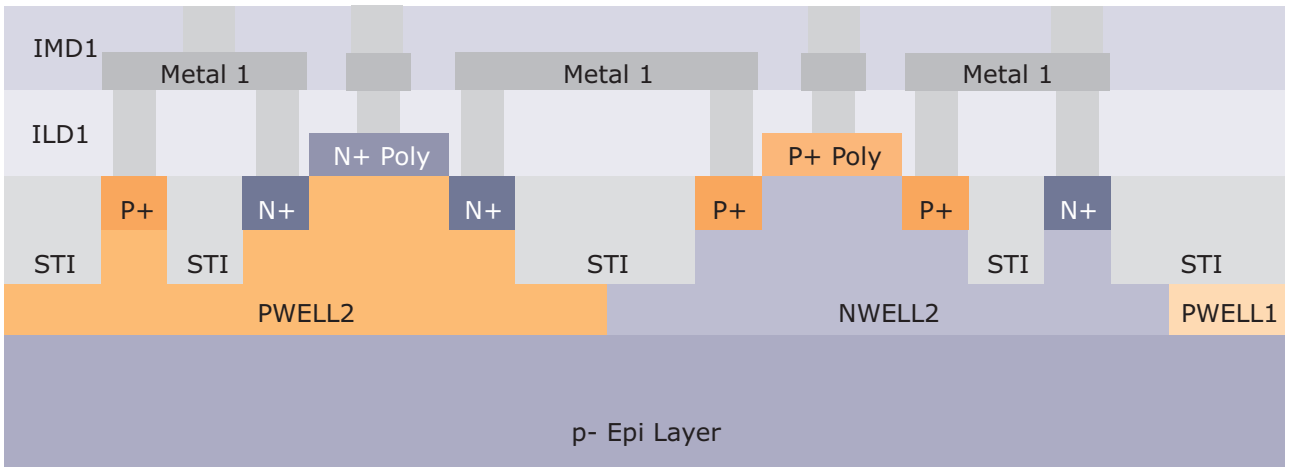
PRIMITIVE DEVICES

- (Isolated) 1.8V, 3.3V LP NMOS/PMOS
- 10V, 15V, 20V, 45V HVMOS, Sym./Asy.
- 35V, 40V, 45V lateral DMOS, isolated
- Depletion NMOS
- Bipolar transistors, ESD protected
- Sandwich, Fringe, MIM Capacitors
- Resistors
- Diffusion, Schottky, Protection, Photo Diodes

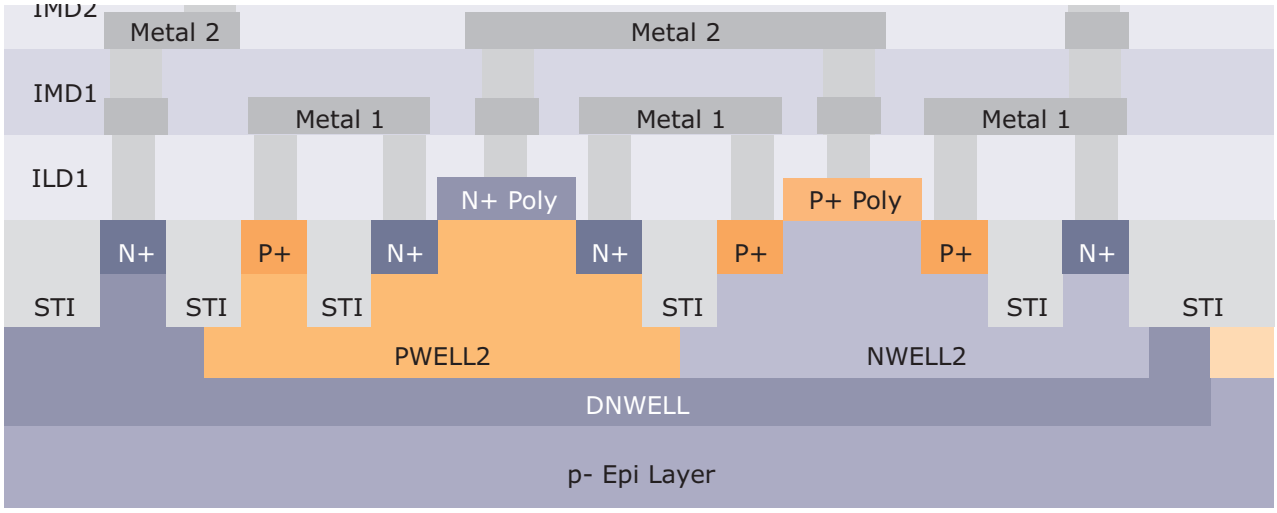
XH018 BASIC DESIGN RULES

Mask	width [µm]	Spacing [µm]
N-well	0.86	1.4
Active Area	0.22	0.28
Poly-silicon Gate	0.18	0.25
Poly-silicon Resistor	0.44	0.44
Contact	0.22	0..25
Metal 1	0.23	0.23
Via 1, 2, 3, 4	0.26	0.26
Metal 2, 3, 4, 5	0.28	0.28
Top Via	0.36	0.35
Top Metal	0.44	0.46
Thick Metal	3.0	2.5

XH018 DEVICES SCHEMATIC CROSS SECTION



ne3 pe3



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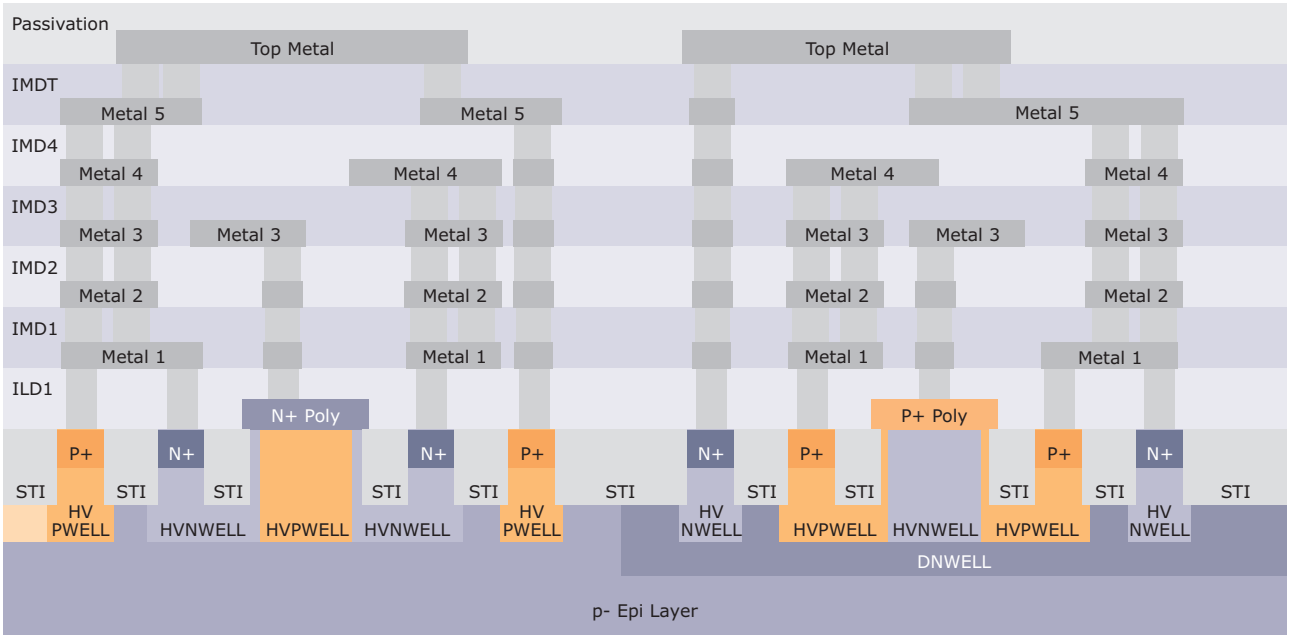


nmma pmma

XH018 PROCESS FLOW

Core Module	Additional Modules		
Wafer Start			
	HV gate oxide	HVMOS	
	Deep HV NWELL	HVPMOS/BIPESD/SCHOTTKY	
Active area			
	Deep N-well	ISOMOS/PHOTODIO/HVMOS	
	HV wells	HVMOS	
	Shallow HV Nwell	NHVE	
	Shallow HV Pwell	PHVE	
	DMOS drift implant	DMOS	
	Depletion implant	DEPL	
	Non volatile memory	NVM, FLASH	
1.8V wells			
3.3V wells			
	1.8V low Vt wells	LVT	
Dual gate oxide			
Poly silicon gate			
Source/Drain implants			
	MRPOLY implant	MRPOLY	
Salicidation			
Contact			
Metal 1			
Via 1			
Metal 2			
	Double MIM capacitor	DMIM/ DMIMH	
	Triple MIM capacitor	TMIM/ TMIMH	
	Via 2 Metal 3	MET3	
	Double MIM capacitor	DMIM/ DMIMH	
	Triple MIM capacitor	TMIM/ TMIMH	
	Via 3 Metal 4	MET4	
	Triple MIM capacitor	TMI/ TMIMHM	
	Via 4 Metal 5	MET5	
	MIM capacitor	MIM/ MIMH	
	Top Via Top Metal	METMID	
	Thick Via Thick Metal	METTHK	
PAD			
	Polyimide deposition	PIMIDE	
			mask steps

XH018 CORE MODULE

Module Name	Descriptions	Masks No.
LPMOS	Low power 1.8V, 3.3V CMOS module	19

XH018 ADDITIONAL MODULES

Module Name	Descriptions	Masks No.
HIGHTEMP	High temperature module	0
LVT	1.8V low Vt module	2
ISOMOS	Triple well isolated CMOS module	1
PHOTODIO	Photo diode module	0
DEPL	Depletion module	1
NVM	Non-volatile-memory module	2
FLASH	Flas module	0
HVMOS	High-voltage module	5
DMOS	DMOS module	1
HVNMOS	HVNMOS module	3
NHVE	High-voltage extension module module	1
HVPMOS	HVPMOS module	6
PHVE	High-voltage extension module	1
BIPESD	ESD module	3
SCHOTTKY	Schottky module	2
OTP3	One-Time Programmable memory module	0
MRPOLY	Medium resistance polysilicon module	1
MIM	MIM capacitor module	1
DMIM	Double MIM capacitor module	1
TMIM	Triple MIM capacitor module	1
MIMH	Single high capacitance MIM capacitor module	1
DMIMH	Double high capacitance MIM capacitor module	1
TMIMH	Triple high capacitance MIM capacitor module	1
MET3	3-metal module	2
MET4	4-metal module	2
MET5	5-metal module	2
METMID	Top metal module	2
METTHK	Thick metal module	2
PIMIDE	Polyimide module	1

XH018 ADDITIONAL MASK COUNT FOR MODULE COMBINATION

Module Name	When combines with modules	Combined additional mask count
HVMOS	ISOMOS	5
HVNMOS	HVMOS	5
HVNMOS	HVPMOS	6
HVNMOS	HVPMOS+HVNE	6
HVPMOS	HVMOS	7
HVPMOS	HVNMOS+PHVE	7
BIPESD	HVMOS	7
SCHOTTKY	HVMOS	6
SCHOTTKY	HVNMOS	4
SCHOTTKY	HVPMOS	6

XH018 RESTRICTION FOR MODULE COMBINATIONS

Module name	Use of the module also requires use of the following module(s)	Use of the module is not available with the use of the following module(s)
LPMOS	MET3+METMID	
HIGHTEMP		PHOTODIO
PHOTODIO	ISOMOS	HIGHTEMP
NVM	ISOMOS	
FLASH	NVM	
DMOS	HVMOS	
NHVE	HVNMOS	
PHVE	HVPMOS	
MIM		DMIM, TMIM, MIMH, DMIMH, TMIMH
DMIM	MET3	MIM, TMIM, MIMH, DMIMH, TMIMH
TMIM	MET4	MIM, DMIM, MIMH, DMIMH, TMIMH
MIMH		MIM, DMIM, TMIM, DMIMH, TMIMH
DMIMH	MET3	MIM, DMIM, TMIM, MIMH, TMIMH
TMIMH	MET4	MIM, DMIM, TMIM, MIMH, DMIMH
MET4	MET3	
MET5	MET4	METTHK
METTHK	METMID	MET5

XH018 METAL OPTIONS

Available Metal Layer Combinations
MET1 - MET2 - MET3 - METTP
MET1 - MET2 - MET3 - MET4 - METTP
MET1 - MET2 - MET3 - METTP - METTPL
MET1 - MET2 - MET3 - MET4 - MET5 - METTP
MET1 - MET2 - MET3 - MET4 - METTP - METTPL

Active Devices

XH018 MOS CORE TRANSISTORS

Device	Name	Available with module	|VT| [V]	IDS [µA/µm]	IOFF [pA/µm]	BVDS [V]	Max. VDS [V]	Max. VGS [V]
1.8V LP NMOS	ne	LPMOS	0.58	475	< 3	> 3.6	1.98	1.98
1.8V LP PMOS	pe	LPMOS	0.65	170	< 3	> 3.6	1.98	1.98
3.3V native Vt NMOS	nn3	LPMOS	0.18	650	-	> 4	3.6	3.6
3.3V LP NMOS	ne3	LPMOS	0.69	615	< 3	> 5.0	3.6	3.6
3.3V LP PMOS	pe3	LPMOS	0.63	315	< 3	> 5.0	3.6	3.6

XH018 LOW VT TRANSISTORS

Device	Name	Available with module	|VT| [V]	IDS [µA/µm]	IOFF [pA/µm]	BVDS [V]	Max. VDS [V]	Max. VGS [V]
1.8V LVT NMOS	nel	LVT	0.33	680	< 30k	> 3.6	1.98	1.98
1.8V LVT PMOS	pel	LVT	0.33	320	< 50k	> 3.6	1.98	1.98

XH018 ISOMOS TRANSISTORS

Device	Name	Available with module	|VT| [V]	IDS [µA/µm]	IOFF [pA/µm]	|BVDS| [V]	max. VDS [V]	max. VGS [V]
Iso. 1.8V LP NMOS, 4T* Iso. 1.8V LP NMOS, 6T*	nei nei_6**	ISOMOS	0.58	475	< 3	> 3.6	1.989	1.98
Iso. 1.8V LP PMOS*	pei	ISOMOS	0.70	170	< 3	> 3.6	1.98	1.98
Iso. 1.8V LVT NMOS, 4T Iso. 1.8V LVT NMOS, 6T Iso. 1.8V LVT NMOS, 6T	neli neli_6** neli_m_6**	ISOMOS+LVT	0.33	680	< 30k	> 3.6	1.98	1.98
Iso. 1.8V LVT PMOS	peli	ISOMOS+LVT	0.33	320	< 50k	> 3.6	1.98	1.98
Iso. 3.3V LP NMOS, 4T* Iso. 3.3V LP PMOS, 6T* Iso. 3.3V LP PMOS, 6T*	ne3i ne3i_6** ne3i_m_6**	ISOMOS	0.69	615	< 3	> 5.0	3.6	3.6
Iso. 3.3V LP PMOS*	pe3i	ISOMOS	0.63	315	< 3	> 5.0	3.6	3.6

* ISOPWELL means PWELL1, PWELL2 or DEPLWELL.
** These devices are variants of the corresponding basic device with underlying wells. Parameters of these devices are identical to the corresponding basic device.

XH018 MEDIUM VOLTAGE TRANSISTORS

Device	Name	Available with module	|VT| [V]	IDS [µA/µm]	RON [kΩ.µm]	RON*A [mΩ.mm²]	BVDSS [V]	Max. |VDS| [V]	Max. VGS [V]
6V NMOS	nma	HVNMOS	1.33	135	3.6	5.5	> 8	6	18
6V PMOS	pma	HVPMOS	1.20	55	13	20	> 8	6	18
10V HV NMOS	nmma	HVMOS	1.55	50	13	62	> 15	10	10
10V Asy. HV NMOS	nmc	NHVE	1.40	80	13	39	> 21	10	18
15V HV PMOS	pmma	HVMOS	1.42	21	41	200	> 20	15	15
15V Sym. HV NMOS	nmmc	NHVE	1.48	41	22	99	> 21	15	18
15V Sym. HV NMOS	nmmd	NHVE	1.62	48	20	112	> 21	15	18
20V Sym. HV PMOS	pmmc	PHVE	1.52	22	54	228	> 21	20	18
20V Asy. HV PMOS	pmc	PHVE	1.29	48	33	92	> 21	20	18

Active Devices (*Continued*)

XH018 HIGH VOLTAGE TRANSISTORS

Device	Name	Available with module	|VT| [V]	IDS [µA/µm]	RON [kΩ.µm]	RON*A [mΩ.mm²]	BVDSS [V]	Max. |VDS| [V]	Max. VGS [V]
45V Sym. HV NMOS	nhhv	NHVE	1.80	68	55	630	> 50	45	18
45V Sym. HV PMOS	phhv	PHVE	1.35	40	101	900	> 51	45	18
45V Asy. HV NMOS	nhv	NHVE	1.65	145	28	181	> 50	45	18
45V Asy. HV PMOS	phv	PHVE	1.30	105	54	269	> 51	45	18

XH018 DMOS TRANSISTORS

Device	Name	Available with module	|VT| [V]	IDS [µA/µm]	RON [kΩ.µm]	RON*A [mΩ.mm²]	BVDSS [V]	Max. |VDS| [V]	Max. VGS [V]
Iso. 40V nLDMOS*	nedi	DMOS	1.6	110	16	60	> 45.5	40	18
35V pLDMOS	ped2	DMOS	2.0	46	42	185	> 40.5	35	18
Iso. 45V nLDMOS	nedia	DMOS	1.6	82	19	114	> 60	45	18
45V pLDMOS	ped	DMOS	1.9	45	48	210	> 50.5	45	18

* 'nedia' is a more robust device with higher on-state drain-source breakdown voltage than 'nedi'

XH018 DEPLETION TRANSISTORS

Device	Name	Available with module	|VT| [V]	IDS [µA/µm]	BVDSS [V]	Max. |VDS| [V]	Max. VGS [V]
3.3V Depl NMOS	nd3	DEPL	0.20	730	> 5	3.6	3.6
Iso. 3.3V Depl NMOS, 4T Iso. 3.3V Depl NMOS, 6T Iso. 3.3V Depl NMOS, 6T	nd3i nd3i_6** nd3i_m_6**	DEPL+ISOMOS*	0.24	740	> 5	3.6	3.6

* The HVMOS module is needed, if isolated MOS transistors are placed in DNWELL instead of DNWELLMV.
** These devices are variants of the corresponding basic device with underlying wells. Parameters of these devices are identical to the corresponding basic device.

XH018 BIPOLAR TRANSISTORS

Device	Name	Available	BETA	VA [V]	BVCEO [V]	VBE [mV]	max. VCE [V]	VEB [V]
1.8V vPNP	qpva qpvb qpvc	LPMOS	2.5 2.6 2.7	> 100		710 669 636	1.98	1.5
3.3V vPNP	qpva3 qpvb3 qpvc3	LPMOS	2.3 2.5 2.5	> 100		709 668 635	3.6	1.5
ESD HV PNP	qpvhscr	BIPESD	28		> 50	580	45	
ESD HV PNP	qpvascr							
3.3V vNPN	qnva	DEPL+HVMOS	> 21	16	> 10	710	3.6	
3.3V vNPN	qnvb	DEPL+ISOMOS	85	8.5	> 4.5	700	3.6	
3.3V vNPN	qnvc	ISOMOS	20	70	> 10	695	3.6	

Passive Devices

XH018 POLY RESISTORS

Device	Name	Available with module	RS [Ω/□]	Temp. Coeff. [10^{-3}/K]	Max VTB [V]
N+ Poly	rnp1 rnp1_3*	LPMOS	330	-1.4	45
P+ Poly	rpp1 rpp1_3*	LPMOS	280	-0.11	45
P+ Poly silicided	rpp1s rpp1s_3*	LPMOS	6.3	2.92	45
High-Ohmic N+ Poly1	rnp1h rnp1h_3*	LPMOS	6700	-5.69	45
Lightly dope P+ Poly1	rpp1k, rpp1k_3*	MRPOLY	1000	-0.9	45

* These devices are variants of the corresponding basic device with an underlying well, but not crossing a well boundry. The models realize an improved description of bulk voltage dependency.

XH018 DIFFUSION RESISTORS

Device	Name	Available with module	RS [Ω/□]	Thickness/junc. depth [µm]	Temp. Coeff. [10^{-3}/K]	Max VTB [V]
1.8V N+ diffusion	rdn	LPMOS	65	0.35	1.42	1.98
1.8V P+ diffusion	rdp	LPMOS	135	0.38	1.23	1.98
1.8V N-well	rnw	LPMOS	940	1.72	2.90	5.5
3.3V N+ diffusion	rdn3	LPMOS	62	0.35	1.42	3.6
3.3V P+ diffusion	rdp3	LPMOS	135	0.38	1.23	3.6
3.3V N-well	rnw3	LPMOS	940	0.58	2.90	5.5
5V Deep N-well	rdnwmv	LPMOS	1500	1.75	5.48	5.5

XH018 METAL RESISTORS

Device	Name	Available with module	RS [Ω/]	Thickness/junc. depth [µm]	Max J/W [mA/µm]	Temp. Coeff. [10^{-3}/K]	Max VTB [V]
Metal 1	rm1	LPMOS	0.095	0.56	0.5*	3.2	45
Metal 2	rm2	LPMOS	0.085	0.56	0.5*	3.2	45
Metal 3	rm3	MET3	0.085	0.56	0.5*	3.2	45
Metal 4	rm4	MET4	0.085	0.56	0.5*	3.2	45
Metal 5	rm5	MET5	0.085	0.56	0.5*	3.2	45
Top Metal	rmtp	METMID	0.043	0.98	1.6*	3.2	45
Thick Metal	rmtpl	METTHK	0.0095	3.00	6**	3.5	45

* value quoted at Tj = -40°C ... +175°C; value for Tj = -40°C ... +125°C is 1.0mA/µm
** value quoted for both Tj = -40°C ... +175°C and Tj = -40°C ... +125°C

Passive Devices (*Continued*)

XH018 SANDWICH CAPACITORS

Device	Name	Available with module	Area Cap [fF]	Max. VTB [V]
Poly1/M1/M2/M3	csandwt3	MET3	0.13	45
Poly1/M1/M2/M3/M4	csandwt4	MET4	0.16	45
Poly1/M1/M2/M3/M4/M5	csandwt5	MET5	0.20	45

XH018 FRINGE CAPACITORS

Device	Name	Available with module	Area Cap [fF]	Voltage Coeff. [1/V]	Max. VTB [V]
Poly1/M1/M2 fringe	csf2p	LPMOS	24.7	-81	45
Poly1/M1/M2/M3 fringe	csf3p	MET3	35.6	-81	45
M1/M2/M3 fringe	csf3	MET3	30.2	24	45
45V M1/M2/M3 fringe	csf3a	MET3	21.7	24	45
M1/M2/M3/M4 fringe	csf4	MET4	40.9	24	45
45V M1/M2/M3/M4 fringe	csf4a	MET4	29.9	24	45
M1/M2/M3/M4/M5 fringe	csf5	MET5	53.0	24	45
45V M1/M2/M3/M4/M5 fringe	csf5a	MET5	38.0	24	45
M1/M2/M3/MTP fringe	csft4	MET3+METMID	34.2	24	45
45V M1/M2/M3/MTP fringe	csft4a	MET3+METMID	26.1	24	45
M1/M2/M3/M4/MTP fringe	csft5	MET4+METMID	45.7	24	45
45V M1/M2/M3/M4/MTP fringe	csft5a	MET4+METMID	34.3	24	45
M1/M2/M3/M4/M5/MTP fringe	csft6	MET5+METMID	57.1	24	45
45V M1/M2/M3/M4/M5/MTP fringe	csft6a	MET5+METMID	42.4	24	45

XH018 MIM CAPACITOR

Device	Name	Available with module	Area Cap [fF/µm²]	V Coeff. [1/V]	|BV| [V]	max. VTB [V]
Single MIM, M3/MTP Single MIM, M4/MTP Single MIM, M5/MTP	cmm4t cmm5t cmm6t	MET3+METMID+MIM MET4+METMID+MIM MET5+METMID+MIM	1.00	15	> 20	45
Double MIM, M2/M3/MTP Double MIM, M2/M3/M4	cdmm4t cdmm4	MET3+METMID+DMIM MET4+DMIM	2.00	3	> 20	45
Triple MIM, M2/M3/M4/MTP Triple MIM, M2/M3/M4/M5	ctmm5t ctmm5	MET4+ METMID+ TMIM MET5+TMIM	3.00	15	> 20	45
High cap. MIM, M3/MTP High cap. MIM, M4/MTP High cap. MIM, M5/MTP	cmmh4t cmmh5t cmmh6t	MET3+METMID+MIMH MET4+METMID+MIMH MET5+METMID+MIMH	2.20	-120	> 10	45
High cap. DMIM, M2/M3/MTP High cap. DMIM, M2/M3/M4	cdmmh4t cdmmh4	MET3+METMID+DMIMH MET4+DMIMH	4.40	-20	> 10	45
High cap. TMIM M2/M3/M4/MTP High cap. TMIM M2/M3/M4/M5	ctmmh5t ctmmh5	MET4+METMID+TMIMH MET5+TMIMH	6.60	-120	> 10	45

Passive Devices (*Continued*)

XH018 PROTECTION DIODES

Device	Name	Available with module	Leakage Current [fA/µm]	|BV|[V]	BV Temp. Coef. [mV/K]	Max Vcc [V]
20V N-type Protection	dnp20	NHVE	300	> 20	10	30
20V P-type Protection	dpp20	HVMOS	100	> 20	18	30

XH018 SCHOTTKY DIODE

Device	Name	Available with module	Vforward [V]	ILeakage [nA/µm]	|BV| [V]	Max. VTB [V]
18V Schottky	dsb	SCHOTTKY	0.45	< 2	> 20	45

XH018 PHOTO DIODES

Device	Name	Available with module	Area dark Current [fA/µm²]	Sensitivity [A/W]	Max Vcc [V]
PD for visible & infrared light detection	dphoa	PHOTODIO	0.040	0.35 / 0.42 / 0.31*	10
PD for infrared light detection	dphob	PHOTODIO	0.038	0.03 / 0.24 / 0.25*	10

** optical responsibility @500nm / @650nm / @850nm

XH018 DIFFUSION DIODE

Device	Name	Available with module	Area Cap [fF/µm²]	|BV| [V]	Leakage Current [fA/µm²]	Max VCC [V]
1.8V N+ diff. /PW	dn	LPMOS	1.12	> 6	5.0×10^{-4}	1.98
1.8V P+ diff. /NW	dp	LPMOS	0.98	> 6	5.0×10^{-4}	1.98
1.8V NW /Psub	dnw	LPMOS	0.12	> 9	1.0×10^{-3}	5.5
3.3V N+ diff. /PW2	dn3	LPMOS	0.87	> 6	7.0×10^{-4}	3.6
3.3V P+ diff. /NW2	dp3	LPMOS	1.00	> 6	7.0×10^{-4}	3.6
3.3V NW /Psub	dnw3	LPMOS	0.12	> 9	1.0×10^{-3}	5.5
P+ diff. /DNW	ddnwmv	ISOMOS	0.08	> 15	5.0×10^{-4}	10
MV DNW /Iso. PW	dipdnwmv	ISOMOS	0.33	> 15	6.0×10^{-4}	3.6
DNW /Psub	ddnw	HVMOS	0.08	> 80	5.0×10^{-4}	40
Iso. PW /MV DNW	dpdnw	HVMOS	0.56	> 10	3.8×10^{-4}	5.5
Iso. PW /DNW	dipdnw	HVMOS	0.33	> 15	6.0×10^{-4}	5.5
N+ diff. /HV PW	dnhpw	HVMOS	0.78	> 9	8.0×10^{-4}	5.5
P+ diff. /HV NW	dphnw	HVMOS	0.68	> 9	2.0×10^{-4}	5.5
HV PW /DNW	dhpw	HVMOS	0.18	> 20	2.5×10^{-4}	15
HV NW /Psub	dhnw	HVMOS	0.11	> 47	2.5×10^{-4}	15
NDF /Psub	dndf	NHVE	0.10	> 50	4.0×10^{-4}	45
PDF /HV NW	dpdwhn	PHVE	0.19	> 50	7.0×10^{-5}	45
HV NW /Psub	dwhn	HVPMOS	0.07	> 50	7.0×10^{-4}	45
P+ diff. /HV NW	dpwhn	HVPMOS	-	> 22	-	20

Non-Volatile-Memory

XH018 POLY FUSE

Device	Name	Available with module	Unprog. Res. [Ω]	Prog. Res. [kΩ]	Prog. Max VT1-T2 [V]	Unprog. Max VT1-T2 [V]
Poly fuse	pfuse	LPMOS	32	> 100	3.6	0.1

XH018 NVM

Parameter	NVRAM Compiler	Flash	TrimOTP Compiler
Available with module	NVM+MIM	NVM+FLASH+MIM	OTP3
Memory Size	1k to 16k bits	8k x32, 16k x32 bits	8 to 16k bits
Operating voltage	1.6 to 2.0V 3.0 to 3.6V	1.6 to 2.0V 3.0 to 3.6V	3.0 to 3.6V
Operating temperature	-40 to +175°C	-40 to +175°C read -40 to +125°C NV write/erase	-40 to +175°C
Endurance	100k cycles for EEPROM @25°C 10k cycles for EEPROM @150°C unlimited SRAM	1k cycles @125°C	
Data retention	Min. 10 years @ 125°C Min 3 year @150°C Min 1 years @175°C	Min. 10 years @125°C Min. 3 years @150°C Min. 1 years @175°C	Min. 20 years @ 125°C
Access time		50ns read, 5ms page write 20ms page erase	55ns read 10ms Byte program

STANDARD CELLS LIBRARIES

XH018 STD CELLS LIBRARY

Device	Library feature	Voltage range	Application benefits
D_CELLS	Standard	1.8V	High speed, P&R competible with D_CELLSL
D_CELLSL	Low power, low leakage	1.8V	Low power consumption, low leakage, P&R compatible with D_CELLS
D_CELLS_JI	Standard, junction isolated	1.8V	Junction isolated, low noise, high speed, voltage shifting
D_CELLS_JI3V	Low power, 3.3V, junction isolated	3.3V	3.3V supply, junction isolated, low leakage, low power consumption, low noise, voltage shifting
D_CELLS_MVJI	Junction isolated, multivoltage, power cut-off	3.3V / 1.8V	3.3V supply, high speed, noise protection, multivoltage , voltage shifting, power cut-off
D_CELLS_MVJI3V	Junction isolated, multivoltage, power cut-off	3.3V / 1.8V	High speed, noise protection, multivoltage , voltage shifting, power cut-off

I/O LIBRARIES

XH018 I/O CELLS LIBRARY

Device	Library Feature	Voltage Range	Application benefits
IO_CELLS_3V	Standard, 3.3V/1.8V multivoltage	1.8V / 3.3V	Pad limited (x < y)
IO_CELLS_F3V	Standard, 3.3V/1.8V multivoltage	1.8V / 3.3V	Core limited (x > y)
IO_CELLS_JI3V	Junction isolated, 3.3V/1.8V multivoltage	1.8V / 3.3V	Junction isolated, pad limited (x < y)

XH018 CIRCUIT UNDER PAD I/O LIBRARY

Process Option	CUP Bond Pad	Layers for CUP wiring
METTHK	METTPL	MET1, MET2, MET3, METTP
MET5	METTP/VIATP/MET4	MET1, MET2, MET3
MET5+METTHK	METTPL	MET1, MET2, MET3, MET4, METTP
MET5+METMID	METTP/VIATP/MET5	MET1, MET2, MET3, MET4

ANALOG LIBRARIES

XH018 3.3V ADC

Name	Principle	Resolutions [Bits]	Accuracy [LSB] INL/DNL	Conversion Time [Clock Cycles]	Conversion Rate [kS/S]	Required Module
aadcc01_3V3	successive approximation	10	1.5 / 0.8	80	80	LPMOS, MIM

Note: All Parameters are valid for VDD: 2.7V to 3.6V, T:-40 ....85°C

XH018 3.3V DAC

Name	Principle	Resolutions [Bits]	Accuracy [LSB] INL/DNL	Conversion Time [µs]	V Ref. [V] (max)	Required Module
adacc01_3v3	voltage scaling	10	1.0 / 0.2	0.5 *	3.3	LPMOS

* @ Vref=3.3V, CL=2pFNote: All Parameters are typical, VDDA: 2.7V to 3.6V, T:-40 ....85°C, VDD: 1.62V to 1.98V

XH018 3.3V BIAS CELLS 1

Name	Bias Voltage VBP for PMOS [V]	Temp. Coeff. IVBP [ppm/°C]	Bias Voltage VBN for NMOS [V]	Temp. Coeff. IVBN [ppm/°C]	Supply Current [µA]	Required Module
abiac01_3v3	VDD-0.725 [1]	±1000	0.80 [2]	±100	0, 5	LPMOS
abiac02_3v3	VDD-0.830 [1]	±2500	0.936 [2]	±2500	4	LPMOS
abiac03_3v3	VDD-0.836 [1]	±2600	0.948 [2]	±2600	20	LPMOS

[1] @VDD=3.3V, T=27°C [2] @VDD=3.3V, T=27°C
Note: All Parameters are typical, VDD: 2.7V to 3.6V, T: -40 ....85°C, all Bias Cells feature a standby mode

XH018 3.3V BIAS CELLS 2

Name	Output Current IOUT [µA]	Temperature Coefficient IOUT [ppm/°C]	Supply Current [µA]	Required Module
acsoc01_3v3	0.21/0.21/0.21/0.21	±1500	0.7	LPMOS
acsoc02_3v3	1.0/2.0/4.0/8.0	±2200	6.3	LPMOS

Note: All Parameters are typical, VDD: 2.7V to 3.6V, T: -40 ....85°C, all Bias Cells feature a standby mode

ANALOG LIBRARIES (*Continued*)

XH018 3.3V COMPARATORS

Name	VICR [V]	TPD for 50mV Overdrive [ns] L->H/H ->L	Conditions CL [pF]; RL [kΩ]	Input Offset Voltage [mV]	Supply Current [µA]	Required modules
acmpc01_3v3	0.0...VDD-1.05	830/880	1.0	< 5	2*	LPMOS
acmpc02_3v3	1.1...VDD-0.1	815/730	1.0	< 5	1.5*	LPMOS
acmpc03_3v3	0.0...VDD (@1µA)	450/460 (@1µA)	1.0	< 5	10 (@1µA)*	LPMOS

* @Tbias = 200nA. Note: All Parameters are typical, VDD: 2.7V to 3.6V, T: -40 ... 85°C, all Comparators feature a standby mode

XH018 3.3V BANDGAP

Name	Bandgap Voltage (unloaded) [V]	Temperature Coeff. [ppm/°C]	Supply Current [µA]	Required Module
abgpc01_3v3	1.232 [1]	±250 [2]	23	LPMOS

[1] @T=27°C, [2] @ T= -40 ... 125°C, Note: All Parameters are typical, VDD: 2.4V to 3.6V, T: -40 ... 125°C, all Bandgaps feature a standby mode

XH018 3.3V POWER ON RESET

Name	DC-Current POR IDDL [µA]	High Vt [V] (typ)	Low Vt [V] (typ)	Delay VDD->H to POR->L TDEL [µs]	Required Module
aporc02_3v3	1.8	2.1	1.9	20	LPMOS
aporc03_3v3	1.8	2.0	2.0	20	LPMOS

Note: All Parameters are valid for VDD: 2.7V to 3.6V, T: -40 ....85°C

XH018 3.3V VOLTAGE REGULATOR

Name	Typ. Output Voltage [V]	Max Output Current [mA]	Line Regulation [mV/V]	Supply Current [µA]	Supply Voltage [V]	Required Module
aregc01_3v3	1.8	20	1; VIN3=2.1 ... 3.6	100	2.4 ... 3.6	LPMOS

Note: All Parameters are valid for T: -40 ....85°C

XH018 3.3V OVER-TEMPERATURE DETECTOR

Name	Temperature Threshold [°C]	Voltage Coefficient of Threshold Temperature [°C/V]; VCTH/VCTL	Low Output Voltage [V]	High Output Voltage [V]	Supply Current [µA]	Required Module
atmpc01_3v3	133	1.2	VSSA	VDDA	35	LPMOS

Note: All Parameters are valid for T: -40 ....85°C

XH018 1.8V BANDGAPS

Name	Bandgap Voltage (unloaded) [V]	Temperature Coeff. [ppm/°C]	Supply Current [µA]	Required Module
abgpc01_1v8	1.219 [1]	-280 ... +130	22	LPMOS
abgpc01_1v8	1.230 [1]	-210 ... +90	22	LPMOS, DEPL, HVMOS

[1] @VDD=-1.8V, T=27°C. Note: All Parameters are typical, VDD: 1.62V to 1.98V, T: -40 ... 125°C, all Bandgaps feature a standby mode

ANALOG LIBRARIES (*Continued*)

XH018 1.8V OPERATIONAL AMPLIFIERS

Name	VOL [V]	VOH [V]	VICR [V]	VIO [mV]	AVD [dB]	B1 [kHz]	SR [V/µs]	PHM [°]	IDD [µA]	max. Load	Required modules
aopac03_1v8	0.02	VDD-0.02	0 ... V_{DD}-0.35	< 5	121	1.16	0.375/0.692	75	255	50pF/50kΩ	LPMOS
aopac04_1v8	0.02	VDD-0.02	0 ... V_{DD}-0.35	< 6	133	3.90	0.685/1.237	80	235	50pF/50kΩ	LPMOS
aopac09_1v8	0.02	VDD-0.02	0 ... V_{DD} 0.65	< 10	105	0.17	0.086/0.047	75	300	50pF/50kΩ	LPMOS
aopac10_1v8	0.02	VDD-0.02	0 ... V_{DD} 0.70	< 10	113	0.40	0.247/0.140	70	180	50pF/50kΩ	LPMOS
aopac11_1v8	0.02	VDD-0.02	0 ... V_{DD}-0.70	< 6	124	1.24	0.994/0.554	68	630	50pF/10kΩ	LPMOS
aopac12_1v8	0.02	VDD-0.02	0 ... V_{DD}-0.70	< 10	140	4.15	3.339/1.930	80	440	50pF/10kΩ	LPMOS

Note: All Parameters are typical, VDD: 2.7V to 3.6V, T: -40 ....125°C, all Opamps feature a standby mode

XH018 1.8V RC OSCILLATORS

Name	Frequency [Hz]	Conditions	Supply Current (specified @ VDD=3.3V, T=25°C) [µA]	Required Module
arcoc01_1v8	1M		3.86	LPMOS
arcoc02_1v8	1M		9.94	LPMOS
arcoc03_1v8	1M	min. VDD=1.2V	18.21	LPMOS
arcoc04_1v8	5M		9.15	LPMOS
arcoc05_1v8	5M		17.56	LPMOS
arcoc06_1v8	5M	min. VDD=1.2V	28.33	LPMOS
arcoc07_1v8	10M		28.36	LPMOS
arcoc08_1v8	20M		43.87	LPMOS
arcoc09_1v8	40M		62.06	LPMOS
arcoc10_1v8	100K		1.23	LPMOS
arcoc11_1v8	200K		1.42	LPMOS
arcoc12_1v8	10K		0.32	LPMOS

Note: Supply voltage: 6-15V. All Parameters are typical, VDD: 1.62V to 1.98V, T: -40 ....125°C

XH018 1.8V BIAS CELLS

Name	Temperature Coefficient IVBP [ppm/°C]	Bias Voltage VBN for NMOS [V]	Supply Current [µA]	Required Module
abiac06_3v3	-2000 ... +1000	0.670*	5	LPMOS
abiac08_3v3	-2000 ... +500	0.710*	20	LPMOS

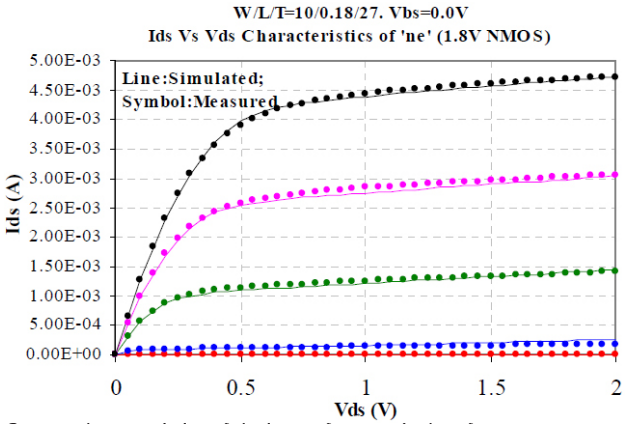
* @VDD=1.8V T=27°C. Note: All Parameters are typical, VDD: 2.7V to 3.6V, T: -40 ....125°C, all Bias Cells feature a standby mode

XH018 1.8V POWER ON/OFF RESET

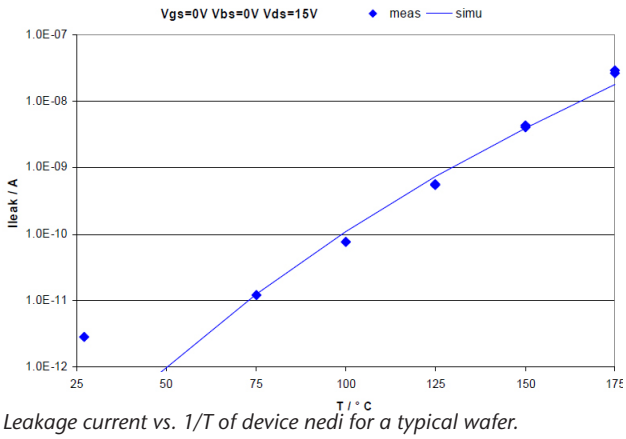
Name	DC-Current POR IDDL [µA]	High Vt [V] (typ)	Low Vt [V] (typ)	Delay VDD->H to POR->L TDEL [µs]	Required Module
aporc02_1v8	2	1.19	1.15	5.07	LPMOS
aporc03_1v8	0.75	1.20	1.17	5.04	LPMOS

Note: All Parameters are valid for VDD: 1.62V to 1.98V, T: -40 ....125°C

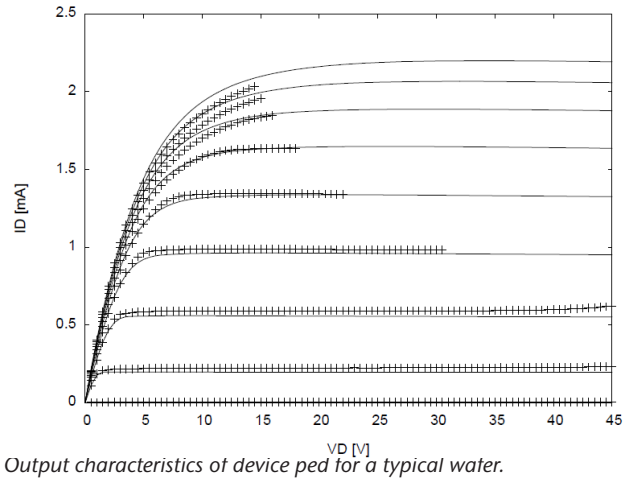
EXAMPLES FOR MEASURED AND MODELED PARAMETER CHARACTERISTICS



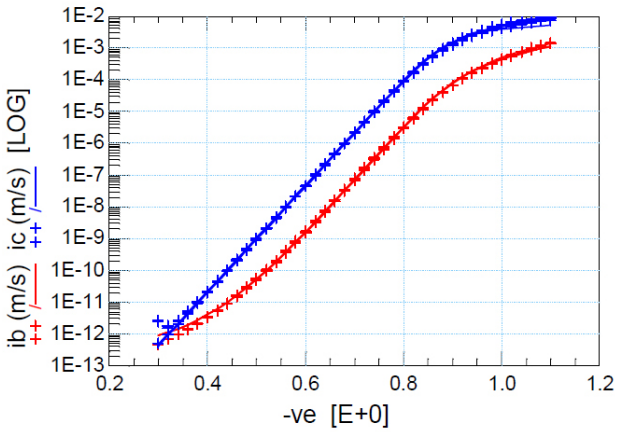
Output characteristics of device ne for a typical wafer,
W/L = 10/0.18, VGS = 0.4, 0.75, 1.10, 1.45, 1.80V, VBS = 0V
symbol = measured, solid line = BSIM3V3 model



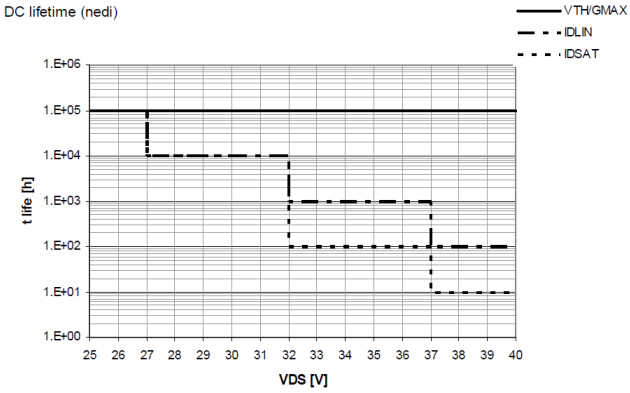
Leakage current vs. 1/T of device nedi for a typical wafer.
W/L = 100/0.65, VGS = VBS = 0V,
symbol = measured, solid line = BSIM3V3 subcircuit model



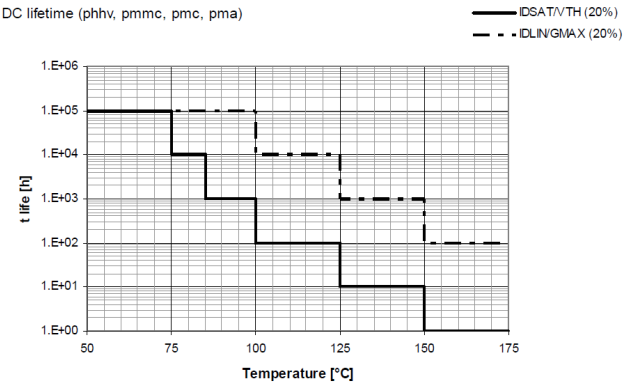
Output characteristics of device ped for a typical wafer.
W/L = 20/5, VGS = 2, 4, 6, 8, 10, 12, 14, 16, 18V,
VS = VB = 0V, symbol = measured, line = HiSIM_HV



Gummel plot of 3.3V vertical HV NPN transistor qnva
for a typical wafer, Emitter length 3.0 µm, VCB = 1, 2, 3V,
symbols = measured values, solid line = VBIC model

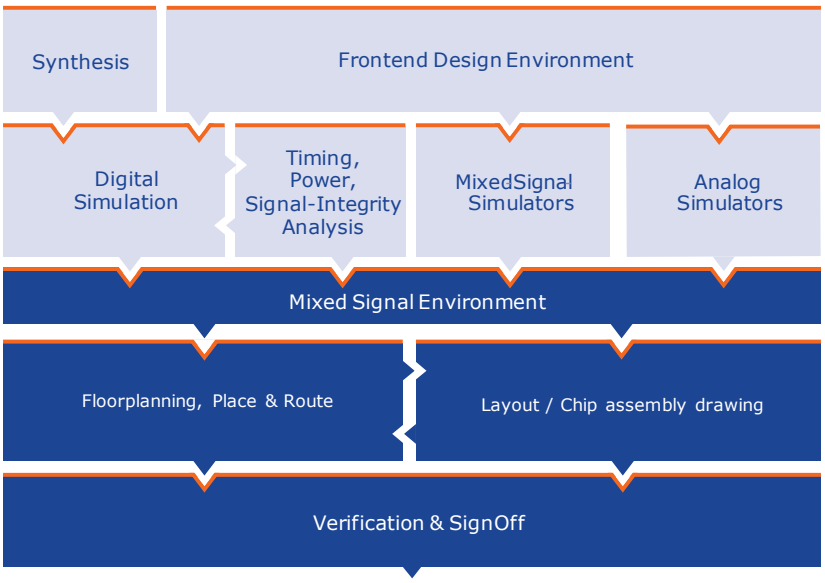


Hot Carrier Injection plot for device nedi for a typical wafer.



Negative Bias Temperature Instability plot for device phhv
for a typical wafer.

XH018 SUPPORTED EDA TOOLS



Note: Diagram shows overview of reference flow at X-FAB. Detailed information of suported EDA tools for major vendors like Cadence, Mentor and Synopsys can be found on X-FAB's online technical information center X-TIC.

X-FAB'S IC DEVELOPMENT KIT "THEKIT"

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