SYNOPSYS®
Silicon to Software™

HAPS Prototyping Solution

Overview

Today's wireless, automotive and industrial products require the combination of multi-processor SoCs and complex software stacks to deliver functionality, power and performance requirements tailored for their target market. The dependency of SoC hardware and software on each other requires a design methodology and development team setup that enables hardware and software to be developed alongside each other. As a result, prototyping has emerged as a key methodology as part of the overall hardware verification, software development and system validation strategy at technology companies.

Synopsys' HAPS® prototyping solution offers an integrated prototyping flow focused on:

- Delivering the highest performance
- Enabling modularity, scalability and real world IO
- Offering the highest debug productivity
- Providing the shortest time to a prototype
- Shifting the entire verification and software development effort left as part of the Synopsys Verification Continuum Platform



Figure 1. HAPS-80 Prototyping Solution

Highest Performance

With the growing complexity and amount of software stacks, the performance of the development platform has become more important than ever. HAPS' unique single-ended high-speed time-domain multiplexing technology supports system routes and transfer of design signals at 1.4 Gbps with a fully integrated and automated prototyping flow. With pre-built prototyping hardware knowledge, HAPS prototyping utilizes extensive industry and customer experience to automatically optimize and efficiently deliver the highest prototype performance, up to 50 MHz for full SoC/Subsystem and 150+ MHz for IP designs.

Modularity, Scalability and Real World IO

With its modular architecture, HAPS systems support IP to SoC system prototyping. Support for real world interfaces through HapsTrak 3 and multi-gigabit PHY daughter cards enables hardware and software validation including host controller and PHY driver validation, interoperability testing and end-to-end performance validation. Multi-Design Mode enables parallel prototyping of multiple design instances on a multi-FPGA HAPS system. The HAPS prototyping cabling flexibility enables optimization for the need of each design, supporting connection of up to 16 HAPS systems. These HAPS systems can be used locally to the end users as desktop system or in a lab, as well as being deployed as part of a prototyping farm, accessible remotely by hardware and software engineers.

Highest Debug Productivity

Prototypes have historically not offered much observability. HAPS prototyping changes the game and addresses the debug needs of hardware and software engineers. Seamless waveform capture across FPGAs and a spectrum of data storage options allow wide access and control with minimal impact to prototyping resources and partition plans.

Shortest Time to Prototype

To maximize actual verification, software development and system validation time, it is important to get to a prototype as quickly as possible. The HAPS prototyping hardware and software were developed together to enable a more automated design preparation, partitioning and synthesis flow. Moreover, the various job flows can be distributed across multiple cores of the host machine to significantly reduce the runtime needed to create the prototyping images.

HAPS-80 offers multiple configurations to support an amplitude of designs.

HAPS-80 Prototyping Solution				
	HAPS-80 S26	**HAPS-80 S52**	**HAPS-80 S104**	**Custom configurations**
ASIC Gate Capacity	26 million	52 million	104 million	Up to 1.6 billion
Number of FPGAs	1	2	4	Up to 64
I/O Connectors HapsTrak 3	24	48	96	Up to 1,536
User Accessible I/O Resources	1084	2465	5086	>81376
Clock Resources	2 PLLs, 2 external PLL inputs, 2x2 external PLL outputs, 2x6 clock input and outputs, frequency ranges: 0.16 - 350 MHz, 367 – 473.33 MHz, and 550 – 710 MHz, clock stopping support			
Debug Storage Options	On-chip BRAM storage, on-FPGA module SDRAM, external SDRAM, or logic analyzer			
Host Interface Option	USB, PCIe-over-cable, or Direct UMRBus API			
Configuration	Ethernet, JTAG, USB 2.0, SD card, UMRBus via Configuration and Data Exchange (CDE) interface			
Power	110-240 AC, 12V			
Compatibility	HAPS-70, HAPS-DX, DesignWare IP Prototyping Kits			
HapsTrak 3 Daughter Boards	Breakout Board, LPDDR3, LPDDR4, DDR3, DDR4, FMC Adapter, GPIO, SRAM HapsTrak II Adapter (USB 3.0, Mobile SDRAM, NOR Flash PROM), Lab Board, Logic Analyzer			
HapsTrak MGB Daughter Boards	10/100/1000 Gigabit Ethernet, Serial ATA, PCI Express Gen 2/3, QSFP+			

Synopsys Verification Continuum

HAPS is a part of the most comprehensive and natively-integrated functional verification ecosystem in the industry. To find SoC bugs earlier and faster, perform software bring-up and validate the entire system, multiple engines are required. Unified Compile with VCS enables a seamless transition between simulation, emulation and prototyping environments. Unified Debug with Verdi increases debug efficiency to find and fix bugs across all domains and abstraction levels.

For more information about Synopsys HAPS prototyping products, support services or training, visit us on the web at: www.synopsys.com/verification/prototyping.html, or contact your local sales representative.

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